Performance Analysis of a New Synchrophasor Based Real Time Voltage Stability Monitoring (RT-VSM) Tool

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Abstract — With the ongoing smart electric grid development, several algorithms and tools have been developed that make use of synchrophasor data for online wide area voltage stability monitoring. Most of these algorithms have several advantages, but at the same time also have limitations. For wide area real time monitoring, there is a need for faster and accurate online voltage stability algorithm. This paper discusses briefly about requirements for online voltage stability monitoring and limitations of few existing approaches. A new algorithm has been presented using a hybrid approach that is not dependent on time series PMU data and at the same time not fully relying on system models. This algorithm has been used to develop the Real Time Voltage Stability Monitoring (RT-VSM) tool to enable system operators in a control center to monitor the wide area voltage stability of a power system. The focus of this paper is investigating the computational performance of the developed algorithm in offline and online environment using simulation platform. Results obtained using the RTVSM tool are presented for different IEEE test cases.

Index Terms — Real time voltage stability tool, wide area voltage stability monitoring, synchrophasor

I. INTRODUCTION

With the ongoing smart grid activities, additional system constraints and increasing complexity, power systems are often being operated closer to the limits. This may result in higher probability of system instability, often characterized by voltage instability and may even lead to a blackout. As numerous voltage instability incidents have occurred around the globe in recent years, more emphasis is being given to perform voltage stability studies in a better way. With the availability of time-synchronized voltage and current phasors, improved algorithms can now be developed to efficiently monitor the voltage stability of a power system [1].

Several voltage stability monitoring approaches have been developed and adopted by the power system researchers and industry members. These algorithms generally aim for static analysis and dynamic analysis, based on the major classification for voltage stability analysis. As part of the static analysis, the information about the distance of the present system operating point from the point of voltage collapse (PoC) is required. Static analysis for voltage stability can be broadly classified into three main approaches:
- Multiple power flow based approach [10]
- Local measurement based approach [2-9,15-17] and
- Decision Tree (DT) based approach [12-14]

Although each of these approaches have their own advantages, they also have some limitations that needs to be addressed. Followings are some of the limitations of these kinds of approaches -

A. Limitations of multiple power flow based static analysis of voltage stability -
(1) Multiple power flow approaches depend largely on mathematical power system models [11]. If the mathematical models are not very accurate in all system conditions, the voltage stability analysis with such an approach may also lead to inaccurate results.

(2) This approach usually involves utilization of current phasor measurements (along with voltage phasors) obtained directly from PMUs installed at the bus. However, it has been seen that the Total Vector Error (TVE) for current phasor estimation by commercial PMUs can be appreciably high [18] that can cause errors in voltage stability margin computation.

B. Limitations of local measurements based static analysis of voltage stability -
(1) Local measurement based approach generally needs a window of past data at the load bus for computation of Thevenin's equivalent parameters of the network as seen from that bus. However, the assumption is that during this windowing period, the system side parameters remain constant whereas the load side parameters keep changing. If the changes in the system side are large in the time window, may be during large load changes or topological changes due to contingencies, the computation of Thevenin's equivalent parameters may not be correct, leading to inaccurate calculation of voltage stability margin.

(2) This approach usually involves utilization of current phasor measurements (along with voltage phasors) obtained directly from PMUs installed at the bus. However, it has been seen that the Total Vector Error (TVE) for current phasor estimation by commercial PMUs can be appreciably high [18] that can cause errors in voltage stability margin computation.

C. Limitations of DT based static analysis of voltage stability -
(1) DTs are trained offline by simulating various scenarios that may occur in a power system and the online application takes decisions based on these trained DTs. Due to the non-linear nature of the power system it is very difficult to predict all the scenarios that might occur and hence the online application may fail to take decisions under those conditions.

(2) The overall prediction behavior of DTs is limited to 90% cases [12], and hence the DTs are set into online learning mode to update when system conditions change. However, this involves running multiple power flows that may be time consuming and not suitable for real time monitoring.

These limitations provide motivation for new voltage stability tool. Details for the conversion of the developed algorithm into an online tool named 'RT-VSM Tool' (coded using C# language and XAML language) for real time wide area voltage stability monitoring has been discussed. A short description of the test bed setup used for real time online simulation of the RT-VSM Tool, followed by discussion of the RT-VSM Tool along with its online results on an IEEE test case has also been provided. A comparative analysis of the timing performance of the online and offline codes for the same algorithm has been presented next. Finally, the conclusion is presented. Unique contribution of this paper is providing details for impact of computational algorithms and implementation using specific software platforms for a new voltage stability tool designed for smart grid operation and control.

II. DEVELOPED REAL TIME VOLTAGE STABILITY MONITORING (RT-VSM) TOOL

A new real time voltage stability monitoring algorithm and software application 'RT-VSM Tool' has been developed and its details are available in [19]. It computes the distance to the point of voltage collapse (PoC) based on a non-iterative method that makes use of wide area voltage phasor measurements and system topological information. The distance to PoC for the load buses in the power system is computed in terms of an index termed 'VSAI' that ranges between '0' and '1', where values near '0' indicate highly voltage stable load bus and values near '1' indicate that the load bus is near the point of voltage collapse. As the developed algorithm is completely non-iterative, it is computationally much less burdensome than the algorithms based on multiple power flow approach. Hence, it has a very short runtime, suitable for real time monitoring of the system voltage stability. It is not highly dependent on the intricate mathematical details of power system models, and hence doesn't get affected by modeling errors. Additionally, unlike the local phasor measurement based approaches, the proposed algorithm does not need a window of time series data for the estimation of voltage stability margin of the load buses. It is also worth mentioning that this algorithm does not use current phasor measurements for computing the distance to voltage collapse point, and thus doesn't get affected when current TVEs of PMUs are very high.

III. PERFORMANCE ANALYSIS OF REAL TIME VOLTAGE STABILITY MONITORING (RT-VSM) TOOL

A. Offline results obtained using the RT-VSM Tool algorithm in MATLAB -

Following subsections provide the results obtained by offline simulation of the developed algorithm -

Case-1: Voltage stability problem in an IEEE-57 Bus test case when loading at all the load buses are increased -

Figure 1 shows the VSAI of all the load buses in the system along with important system metrics for the base case. It can be seen that the VSAI of the weakest bus in the system at base case is that of Bus-47 (VSAI = 0.5579). The loading at all the load buses is now increased maintaining the same power factor at each bus, and considering PV-PQ switching, unless the power flow fails to converge. Figure 2 shows the VSAI along with the key system metrics during this stressed condition. It can be seen that, the voltage magnitudes at the buses have decreased, voltage angular separation of buses have increased and the VSAI of all the load buses have increased, with the weakest bus in the entire system being Bus-31 (VSAI = 0.8014), which exceeds the set VSAI alarm limit of 0.8 (alarm limit preferred by the user for required voltage stability margin based on baselining studies).

Figure 1. Key system metrics at base case

Figure 2. Key system metrics at stressed case
Case-2: Voltage stability problem in an IEEE-57 Bus test case with a line contingency

Figure 3 shows the VSAI of all the load buses in the system along with important system metrics for base case system. However, if a fault at line 46-47 causes this line to be taken out of the system, then this stresses the system as indicated by the increase in the VSAI at Bus-47 from 0.5579 to 0.6212. As the VSAI alarm value has been set at 0.6 for this specific case, hence figure-3 shows that Bus-47 VSAI has exceeded this alarm limit.

From the presented offline results, it can be concluded that system wide VSAI computation by the newly developed algorithm can give the control center operators a clear view of voltage stability margins of all the load buses in the monitored system, as the VSAI values are qualitatively in accordance with the analytical theory of small disturbance and large disturbance voltage stability problems.

B. Online results obtained using the RT-VSM Tool & a Real Time Test Bed -

Figure 4 shows the schematic representation of the online setup for testing of the proposed real time voltage stability algorithm on an IEEE 14 Bus test case. A different test case is chosen here to give emphasis to the performance analysis of the RT-VSM tool.

The first stage in the setup consists of building a power system test case for which the voltage stability needs to be monitored in real time using RSCAD modeling, which is the interfacing software for the Real Time Digital Simulator (RTDS) [20]. The built test case is downloaded in the RTDS that runs on parallel processing technology to compute the electrical parameters at all the buses in this system in real time (with a time step of 50 µs) and also generates analog and digital signals. There are number of hardware PMU’s connected to RTDS from several different vendors.

The RTDS also has a GTNET PMU card that can emulate 8 PMUs, and provides instantaneous voltage and current analog signals on a reduced scale. The 8 GTNET PMUs in the RTDS will have the same IP address and different Device IDs. However, in reality the PMUs at different substations will have different IP addresses. To imitate this realistic situation, a Phasor Data Concentrator (PDC-1) is used to concentrate the data of all the GTNET PMUs and the hardware PMUs at each substation. PDC also split them up into virtual PMUs that can be located strategically in the different substations.

The required numbers of PMUs are located at the substations to measure the voltage phasors. To make the test setup closer to reality, communication issues like data latency and packet dropping are simulated using a network simulator NS3 [21]. The data from all the segregated PMUs that come to the control center through the communication emulator is...
aggregated in another PDC-2 that replicates a Super PDC. The PDC-2 accumulates and streams data according to C37.118 Standard protocol [22], and hence a protocol converter interface is built in C# so as to stream in data from the PDC-2 into the voltage stability monitoring tool built using the developed wide area algorithm. More details on the real time test bed setup and its capabilities can be found in [23, 24].

C# Language and XAML have been used to build the RT-VSM Tool. The test bed setup discussed earlier has been used to monitor the system voltage stability of the IEEE-14 test case in real time using RT-VSM Tool, the results of which are shown below. Note that real time simulation results are presented only for small system IEEE 14 bus as limited by RTDS hardware capabilities. Although developed tool can be used for much bigger system and further investment in RTDS hardware will enable that.

Figure 5 and figure 7 show the main visualization dashboard of the RT-VSM Tool for the IEEE-14 bus test case during base case. It can be seen that Bus-9 is the weakest bus with VSAI of 0.44, but this is much lesser than the VSAI alarm limit of 0.9 (alarm limit preferred by the user for required voltage stability margin based on baselining studies). Figure 6 and figure 8 show the critical system metrics visualization windows of the RT-VSM Tool that is monitoring the test power system with load increase at all the load buses (until the power flow fails to converge). The figures show that during the stressed case, VSAI of all the load buses increase. It is found that buses 9 and 14 have VSAI values above the set alarm value of 0.9, as has been indicated in figure 6 (by showing the stressed buses in red color) as well as in figure 8 (by showing the VSAI values of the stressed buses).
C. Comparison of timing performance of the developed algorithm / tool -

The real time voltage stability tool has been developed and tested both offline and online. Two types of comparisons have been made -

1. Timing performance comparison in the same computer:
The specification of the computer used for this test is -
Computer: 2.1 GHz, Dual Core

Figure 9 shows the results of comparison of timing performance of the RT-VSM Tool algorithm in the form of its computation time-step (i.e. time required to run the algorithm once) using MATLAB (offline) and C# & XAML (online) on the specified computer. It can be seen very clearly that when C# & XAML is used, the timing performance of the algorithm improves drastically for systems of different sizes (i.e. IEEE-14 Bus, 30 Bus, 57 Bus and 118 Bus test systems).

2. Timing performance comparison on different computer configurations for online simulation (using algorithm code in C# and XAML):
The specification of the computers used for this test is -
Computer 1: 2.1 GHz, Dual Core
Computer 2: 2.8 GHz, Quad Core

Figure 10 shows the timing performance comparison of the RT-VSM Tool algorithm in the form of its computation time-step when it is run online on 2 different computers with different configurations. It can be very clearly seen that computer configuration has a noticeable impact on the online timing performance of RT-VSM Tool. The higher end computer configuration significantly reduces the algorithm time step for all the test cases (i.e. IEEE-14 Bus, 30 Bus, 57 Bus and 118 Bus test systems).
IV. CONCLUSIONS

In this paper, performance analysis of the newly developed wide area voltage stability for a smart grid has been presented. The motivation behind the development of a new wide area real time voltage stability monitoring algorithm / tool has also been presented. Two aspects of the performance of the developed algorithm discussed here are accuracy performance and timing performance. The offline results presented in this paper show the accuracy of the proposed algorithm in detecting small disturbance voltage stability problems also large disturbance voltage stability problems. The test bed setup required for online implementation of the RT-VSM Tool has been discussed, followed by the online results obtained by using this tool in real time. The timing performance of the algorithm / tool has also been tested for different software platform as well as on different computer configurations. It can be seen that both these factors, i.e. software platform and host computer configuration have a noticeable effect on the runtime performance of the RT-VSM Tool.

V. REFERENCES


VI. BIOGRAPHIES

Saugata S. Biswas (S’12) received his B.E. degree in Electrical Engineering from Nagpur University, Nagpur, India, in 2007. He is the recipient of several Gold Medal awards from Nagpur University for his academic achievements during 2003-2007. He worked in the Design and Development Department of a Switchgear industry in India from 2007 to 2009. From 2009 to 2010, he was in the Mississippi State University as a PhD student. From 2011, he is continuing as a PhD student at Washington State University. He is the recipient of the 2013 EEEC Outstanding PhD Student in Electrical Engineering award from Washington State University, Pullman. His research interests include real time monitoring and control of power systems using synchrophasor technology, synchrophasor device testing, and substation automation for online health monitoring of substations devices.

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